

# CURRICULUM VITAE

## **Love Kumar Sah, Ph.D.**

Assistant Professor, Electrical & Computer Engineering  
Western New England University (WNEU), Springfield, MA

Email: [love.sah@wne.edu](mailto:love.sah@wne.edu)

[Google Scholar](#)

---

## **EDUCATION**

**Ph.D., Computer Science & Engineering**, University of South Florida (USF), 2020

**Dissertation:** *Micro-architectural Countermeasures for Control Flow and Misspeculation-Based Software Attacks*

**M.S., Computer Engineering**, University of South Florida, 2016

**M.Sc., Computer System & Knowledge Engineering**, Tribhuvan University, 2013–2014  
(Credits transferred to USF)

**B.E., Computer Engineering**, Tribhuvan University, 2009

---

## **ACADEMIC APPOINTMENTS**

**Assistant Professor**, Electrical & Computer Engineering, WNEU, 2021–Present

**Graduate Teaching Assistant**, University of South Florida, 2014–2020

**Lecturer**, Khwopa College of Engineering, Tribhuvan University, 2010–2014

---

## **RESEARCH INTERESTS**

Hardware Security & Trust • LLM-Assisted Firmware Analysis • AI-Guided EDA Optimization

---

## **INSTRUCTOR OF RECORD**

### **Western New England University**

- CPE491/591: ST: AI & Intelligent System Design(S26)
- CPE490/590: ST: Computer System Security & Trust (W21, F25)
- CPE490/590: ST: Digital Design Optimization & Verification (F23)
- CPE462/562: VHDL: Simulation & Synthesis (S21, S22, S23, S24, S25)
- CPE305: Data Structures for Firmware Design (F21–F25)
- EE285: C Programming (S22–S25)
- CPE271: Digital System Design (S22–S25)
- EE205: Electrical Engineering I (F22-F25)

### **University of South Florida**

- CDA4205: Computer Architecture (Su17, Su18)
- CDA3103: Computer Organization (Su16)

### **Tribhuvan University**

- CT603: Computer Organization & Architecture (S10–S14)

- EX511: Microprocessors (S10–S14)
  - CT501: Object-Oriented Programming (F10–F13)
  - CT401: Computer Programming (F10–F13)
- 

## **GRANTS & FUNDING**

- **NSF Student Participation Grant – MWSCAS 2024**, Lead PI, \$30,000 (2024)
  - **NSF SaTC-EDU Grant- Workforce Development Program for Careers in AI and Cybersecurity**, Co-PI, \$600,000 (under review/hold)
  - **Altera FPGA Equipment Grant**, \$4500 Intel/Altera 2021
- 

## **AWARDS & HONORS**

- **Best Paper Nomination**, AsianHOST 2018
  - **Best Poster Winner**, USF Graduate Research Symposium, 2018
  - **Winner**, USF Engineering Graduate Research Symposium (2 of 52 presentations), 2018
  - **A. Richard Newton Young Student Fellow Award**, Design Automation Conference (DAC), 2017
- 

## **UNIVERSITY & COLLEGE SERVICE**

### **Western New England University**

- College of Engineering Awards Committee (2023–Present)
- ECE Faculty Search Committee (2022)
- WNEU University Diversity Inclusion Committee Member 2025
- College Representative, FIRST Robotics Competition (Western MA Region)

### **Tribhuvan University**

- Exam Coordinator, Khwopa College of Engineering (2011–2014)
- 

## **PROFESSIONAL SERVICE**

### **Leadership Roles**

- **Student Affairs Chair**, IEEE MWSCAS 2024
- **Poster Session Chair**, IEEE SATC 2025
- **Special Session Chair/ Organizer**: “Secure and Trustworthy Cyberinfrastructure for IoT and Microelectronics”, IEEE Midwest Symposium on Circuits and Systems 2021, 2024, 2025 (2025 Co-chair - Prof., Aatmesh Shrivastava, Northeastern University, Boston)

### **Technical Program Committees**

- **TPC Member**, IEEE ISVLSI 2021
- **TPC Member**, IEEE SATC 2025

### **Reviewer**

- IEEE Transactions on Parallel and Distributed Systems (TPDS)
- IEEE Transactions on Emerging Topics in Computing (TETC)
- IEEE Transactions on Dependable and Secure Computing (TDSC)

- IEEE International Conference on Computer Design (ICCD) 2025
- IEEE GLSVLSI (2018–2020)
- IEEE VLSI-SoC (2017)
- IEEE MWSCAS (2018–2025)
- IEEE ISQED (2023)

### **Professional Memberships**

- Member, **ACM, IEEE**
- Active Member, **New England Hardware Security Consortium**
- Active Member, **KEEN Network**
- **Vice President**, IEEE Computer Society USF Student Chapter, 2018

---

### **PEER-REVIEWED PUBLICATIONS**

#### **Journal Articles**

[J1] S. A. Islam, **L. K. Sah**, and S. Katkooori, “**High-level synthesis of key-obfuscated RTL IP with design lockout and camouflaging**,” *ACM Trans. Des. Autom. Electron. Syst.*, vol. 26, Oct. 2020.

[J2] S. A. Islam, **L. K. Sah**, and S. Katkooori, “**A framework for hardware Trojan vulnerability estimation and localization in RTL designs**,” *J. Hardware Syst. Security*, pp. 246–262, 2020.

---

#### **Conference Papers**

[C1] A. Ghimire, G. Ghajari, K. Gurung, **L. K. Sah**, and F. Amsaad, “**Enhancing cybersecurity in critical infrastructure with LLM-assisted explainable IoT systems**,” in *Proc. 1st IEEE Conf. Secure and Trustworthy CyberInfrastructure for IoT and Microelectronics (SaTC)*, Dayton, OH, USA, 2025.

[C2] S. K. Sah and **L. K. Sah**, “**Variable Record Table: A unified hardware-assisted framework for runtime security**,” in *Proc. 68th IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Lansing, MI, USA, 2025.

[C3] S. Khaled, **L. K. Sah**, and F. Amsaad, “**The art of obfuscation: A comprehensive survey of software protection techniques**,” in *Proc. 1st IEEE Conf. Secure and Trustworthy CyberInfrastructure for IoT and Microelectronics (SaTC)*, Dayton, OH, USA, 2025 (to appear).

[C4] S. K. Sah and **L. K. Sah**, “**VRT: A runtime protection against back-edge CFI violation**,” in *Proc. 67th IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Springfield, MA, USA, 2024.

[C5] **L. K. Sah**, S. A. Islam, and S. Katkooori, “**Defending misspeculation-based cache probe attacks using Variable Record Table**,” in *Proc. 21st IEEE Int. Symp. Quality Electron. Design (ISQED)*, Santa Clara, CA, USA, 2021, pp. 408–413.

[C6] **L. K. Sah**, S. Polnati, S. A. Islam, and S. Katkooori, “**Basic block encoding based run-time CFI check for embedded software**,” in *Proc. 28th IEEE Int. Conf. Very Large Scale Integration (VLSI-SoC)*, Salt Lake City, UT, USA, 2020, pp. 135–140.

- [C7] S. A. Islam, **L. K. Sah**, and S. Katkooori, “**Analytical estimation and localization of hardware Trojan vulnerability in RTL designs**,” in *Proc. 20th IEEE Int. Symp. Quality Electron. Design (ISQED)*, Santa Clara, CA, USA, 2020, pp. 149–154.
- [C8] **L. K. Sah**, S. A. Islam, and S. Katkooori, “**Variable Record Table: A runtime solution for mitigating buffer overflow attack**,” in *Proc. 62nd IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Dallas, TX, USA, 2019, pp. 239–242.
- [C9] S. A. Islam, **L. K. Sah**, and S. Katkooori, “**DLockout: A design lockout technique for key-obfuscated RTL IP designs**,” in *Proc. 5th IEEE Int. Symp. Smart Electronic Systems (iSES)*, Rourkela, India, 2019, pp. 17–20.
- [C10] **L. K. Sah**, S. A. Islam, and S. Katkooori, “**An efficient hardware-oriented runtime approach for stack-based software buffer overflow attacks**,” in *Proc. IEEE Asian Hardware Oriented Security and Trust Symp. (AsianHOST)*, Hong Kong, 2018, pp. 1–6. (**Best Paper Nomination**)
- [C11] S. A. Islam, **L. K. Sah**, and S. Katkooori, “**Empirical word-level analysis of arithmetic module architectures for hardware Trojan susceptibility**,” in *Proc. IEEE Asian Hardware Oriented Security and Trust Symp. (AsianHOST)*, Hong Kong, 2018, pp. 109–114.
- 

#### **ACADEMIC PRESENTATIONS**

1. “**Architectural Support for Detecting Software Attacks on IoT Edge Processors**,” Warren B. Nelms IoT Conference, Gainesville, FL, 2019.
  2. “**Architectural Support for Detecting Software Attacks on IoT Edge Processors**,” Florida Center for Cybersecurity (FC2), Tampa, FL, 2018.
  3. “**Architectural Support for Mitigating Buffer-Overflow Attacks**,” USF Graduate Research Symposium, 2018 (Winner).
  4. “**ASIP Synthesis: A Survey**,” Design Automation Conference (DAC), Austin, TX, 2017.
- 

#### **Master’s Thesis Advising**

- *Nittala Srinivas* “**Side Channel Analysis of Modern Cryptographic Processors**”, 2025, Western New England University.